Amendments to the Claims:

1-14. (Canceled).

15. (Currently Amended) A semiconductor apparatus containing a ~~low~~ lower potential reference circuit region and a ~~high~~ higher potential reference circuit region between which signals are transmitted, the signals at the lower potential reference circuit region having a potential lower than the signals at the higher potential reference circuit region, the semiconductor apparatus comprising:

a substrate region;

an epitaxial layer provided on the substrate region;

a high withstand voltage separating region formed in the epitaxial layer, which is arranged between the low and high potential reference circuit regions ~~and~~ separating the lower potential reference circuit region from the higher~~both~~ potential reference circuit ~~regions~~region;

a relay semiconductor device, formed in a doped region of the high withstand voltage separating region in the epitaxial layer, for transmitting a signal from one of the low and high potential reference circuit regions to the other of them, wherein the potential at the lower potential reference circuit region is lower than the potential at the higher potential reference circuit region; and

an insulating partition arranged ~~at least~~ between the relay semiconductor device and one of the low and high potential reference circuit regions that is at ~~the~~ an output ~~one~~ of the relay semiconductor device, the insulating partition being filled with insulating material in a trench extending to the substrate region and partitioning the epitaxial layer to separate the relay semiconductor device from the low potential reference circuit and the high potential reference circuit,

wherein output wiring of the relay semiconductor device is wired to an output of at least one of the low and high potential reference circuit regions bridging over the insulating partition.

16. (Currently Amended) A semiconductor apparatus according to claim 15 ~~further comprising a~~ wherein the substrate region arranged below the ~~low~~ lower and ~~high~~ higher potential reference circuit regions, wherein

bottom portion of the insulating partition extends to the substrate region, and

the insulation partition surrounds the relay semiconductor device.

17. (Currently Amended) A semiconductor apparatus according to claim 15 ~~further comprising~~ wherein the insulating partition comprises a group of insulating partitions arranged between the ~~low~~ lower and ~~high~~ higher potential reference circuit regions, the group of insulating partitions dividing space between the ~~low~~ lower and ~~high~~ higher potential reference circuit regions into plural regions.

18. (Currently Amended) A semiconductor apparatus according to claim 16 ~~further comprising~~ wherein the insulating partition comprises a group of insulating partitions arranged between the ~~low~~ lower and ~~high~~ higher potential reference circuit regions, the group of insulating partitions dividing space between the ~~low~~ lower and ~~high~~ higher potential reference circuit regions into plural regions.

19. (Currently Amended) A semiconductor apparatus according to claim 15,

wherein the high withstand voltage separating region surrounds one of the ~~low~~ lower and ~~high~~ higher potential reference circuit regions,

a plurality of the relay semiconductor devices are arranged to form a ring shape in the high withstand voltage separating region,

each relay semiconductor device is surrounded with the insulating partition, and

output wiring of each relay semiconductor device is wired to at least one ~~an~~ output ~~one~~ of either the ~~low~~ lower potential reference circuit region ~~and~~ or the ~~high~~ higher potential reference circuit ~~regions~~ region bridging over the insulating partition.

20. (Currently Amended) A semiconductor apparatus according to claim 15 further comprising:

[[a]]wherein the substrate region is arranged below the ~~low~~ lower and ~~high~~ higher potential reference circuit regions; and

an insulating layer embedded between the ~~low~~ lower and ~~high~~ higher potential reference circuit regions and the substrate region, the insulating layer electrically insulating the ~~low~~ lower and ~~high~~ higher potential reference circuit regions from the substrate region,

wherein bottom portions of the insulating partitions extend to the insulating layer and the insulating partitions surround the relay semiconductor devices.

21. (Currently Amended) A semiconductor apparatus according to claim 19 further comprising:

[[a]]wherein the substrate is region arranged below the ~~low~~ lower and ~~high~~ higher potential reference circuit regions; and

an insulating layer embedded between the ~~low~~ lower and ~~high~~ higher potential reference circuit regions and the substrate region, the insulating layer electrically insulating the ~~low~~ lower and ~~high~~ higher potential reference circuit regions from the substrate region,

wherein bottom portions of the insulating partitions extend to the insulating layer and the insulating partitions surround the relay semiconductor device.

22. (Currently Amended) A semiconductor apparatus according to claim 15 comprising:

[[a]]wherein the substrate region is formed from semiconductor materials of a first conduction type;

wherein the ~~low~~ lower and ~~high~~ higher potential reference circuit regions are regions formed from semiconductor materials of a second conduction type formed over a main surface of the substrate region so that one of either the

lower potential reference circuit region or the higher potential reference circuit region regions surrounds and is separated from the other ~~in separated relation~~, and

the high withstand voltage separating region is a region formed in a ring shape between the ~~low~~ lower and ~~high~~ higher potential reference circuit regions.

23. (Currently Amended) A semiconductor apparatus according to claim 15 further comprising:

[[a]]wherein the substrate region ~~of~~ is formed from semiconductor materials of either a first or a second conduction type; and

an insulating film formed on the substrate region;

wherein the ~~low~~ lower and ~~high~~ higher potential reference circuit regions are regions of second conduction type formed on the insulating film so that one of the regions surrounds and is separate from the other ~~in separated relation~~, and

the high withstand voltage separating region ~~is~~ includes a region formed in a ring shape between the ~~low~~ lower and ~~high~~ higher potential reference circuit regions.

24. (Currently Amended) A semiconductor apparatus according to claim 22, wherein

a bottom portion of the insulating partition extends to the substrate region, and

the insulating partition surrounds a periphery of the[[a]] relay semiconductor device from at least three directions.

25. (Currently Amended) A semiconductor apparatus according to claim 23, wherein

a bottom portion of the insulating partition extends to the insulating film, and

the insulating partition surrounds a periphery of the[[a]] relay semiconductor device from at least three directions.

26. (Currently Amended) A semiconductor apparatus according to claim 22, wherein the high withstand voltage separating region composes junction isolation-type structure in which high withstand voltage is maintained by a PN junction.

27. (Currently Amended) A semiconductor apparatus according to claim 23, wherein the high withstand voltage separating region composes junction ~~isolation-type~~ isolation-type structure in which high withstand voltage is maintained by a PN junction.

28. (Currently Amended) A semiconductor apparatus according to claim 22, wherein the high withstand voltage separating region has insulation isolation-type structure in which high withstand voltage is maintained by a plurality of insulating partitions.

29. (Currently Amended) A semiconductor apparatus according to claim 23, wherein the high withstand voltage separating region has insulation isolation-type structure in which high withstand voltage is maintained by a plurality of insulating partitions.

30. (Currently Amended) A semiconductor apparatus according to claim 28, wherein

regions partitioned by the plurality of insulating partitions within the high withstand voltage separating region have a capacitor structure in which the plurality of insulating partitions works as dielectric film, and

potential elevates gradually from the ~~low~~ lower potential reference circuit region toward the ~~high~~ higher potential reference circuit region.

31. (Currently Amended) A semiconductor apparatus according to claim 29, wherein

regions partitioned by the plurality of insulating partitions within the high withstand voltage separating region have a capacitor structure in which the plurality of insulating partitions works as dielectric film, and

potential elevates gradually from the ~~low~~ lower potential reference circuit region toward the ~~high~~ higher potential reference circuit region.

32. (Currently Amended) A semiconductor apparatus according to claim 15 further comprising:

[[a]]the substrate region is formed from semiconductor materials of a first conduction type;

wherein the ~~low~~ lower and ~~high~~ higher potential reference circuit regions are regions formed from semiconductor materials of a second conduction type formed on a main surface of the substrate region so that one of either the lower potential reference circuit region or the higher potential reference circuit region regions surrounds and is separated from the other ~~in separated relation~~, and

the relay semiconductor device comprises a plurality of relay semiconductor devices are arranged to form a ring shape in the high withstand voltage separating region.

33. (Currently Amended) A semiconductor apparatus according to claim 15 further comprising:

[[a]]wherein the substrate region ~~of~~ is formed from semiconductor materials either a first or a second conduction type; and

an insulating film formed on the substrate region;

wherein the ~~low~~ lower and ~~high~~ higher potential reference circuit regions are regions of second conduction type formed on the insulating film so that one of the regions surrounds and is separate from the other ~~in separated relation~~, and

the relay semiconductor device comprises a plurality of relay semiconductor devices are arranged to form a ring shape in the high withstand voltage separating region.

34. (Currently Amended) A semiconductor apparatus according to claim 32, wherein

a bottom portion of the insulating partition extends to the substrate region, and

the insulating partition surrounds a periphery of the [[a]] relay semiconductor device from at least three directions.

35. (Currently Amended) A semiconductor apparatus according to claim 33, wherein

a bottom portion of the insulating partition extends to the insulating film, and

the insulating partition surrounds a periphery of the [[a]] relay semiconductor device from at least three directions.

36. (Currently Amended) A semiconductor apparatus according to claim 19 comprising:

[[a]]the substrate region is formed from semiconductor materials of a first conduction type,

wherein the ~~low~~ lower and ~~high~~ higher potential reference circuit regions are regions formed from semiconductor materials of a second conduction type formed over a main surface of the substrate region so that one of either the lower potential reference circuit region or the higher potential reference circuit region regions surrounds and is separate from the other ~~in separated relation~~.